LTC1863/LTC1867

12-/16-Bit, 8-Channel 200ksps ADCs

FEATURES

- **Sample Rate: 200ksps**
- **16-Bit No Missing Codes and ±2LSB Max INL**
- **8-Channel Multiplexer with:**
  Single Ended or Differential Inputs and
  Unipolar or Bipolar Conversion Modes
- **SPI/MICROWIRE™ Serial I/O**
- **Signal-to-Noise Ratio: 89dB**
- **Single 5V Operation**
- **On-Chip or External Reference**
- Low Power: 1.3mA at 200ksps, 0.76mA at 100ksps
- Sleep Mode
- Automatic Nap Mode Between Conversions
- 16-Pin Narrow SSOP Package

APPLICATIONS

- Industrial Process Control
- High Speed Data Acquisition
- Battery Operated Systems
- Multiplexed Data Acquisition Systems
- Imaging Systems

DESCRIPTION

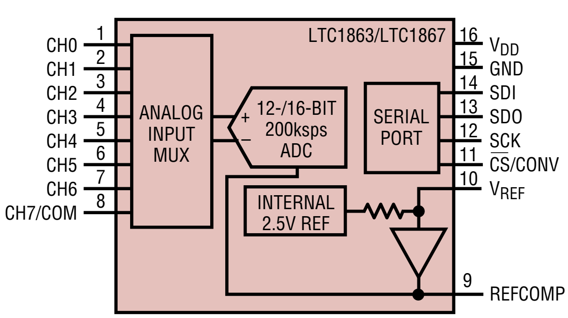
The LTC®1863/LTC1867 are pin-compatible, 8-channel 12-/16-bit A/D converters with serial I/O, and an internal reference. The ADCs typically draw only 1.3mA from a single 5V supply.

The 8-channel input multiplexer can be configured for either single-ended or differential inputs and unipolar or bipolar conversions (or combinations thereof). The automatic nap and sleep modes benefit power sensitive applications.

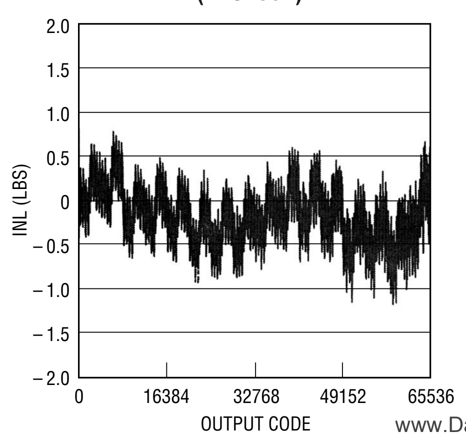
The LTC1867's DC performance is outstanding with a ±2LSB INL specification and no missing codes over temperature. The signal-to-noise ratio (SNR) for the LTC1867 is typically 89dB, with the internal reference.

Housed in a compact, narrow 16-pin SSOP package, the LTC1863/LTC1867 can be used in space-sensitive as well as low-power applications.

BLOCK DIAGRAM



Integral Nonlinearity vs Output Code (LTC1867)

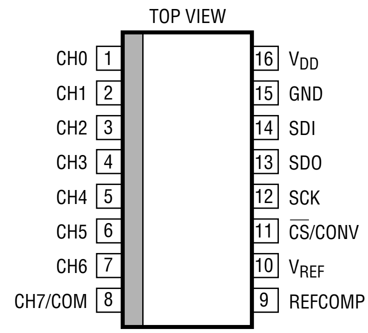


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) .... –0.3V to 6V
Analog Input Voltage
  CH0-CH7/COM (Note 3) .... –0.3V to (V_{DD} + 0.3V)
  V_{REF}, REFCOMP (Note 4) .... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage (SDI, SCK, $\overline{CS}$/CONV)
  (Note 4) .... –0.3V to 10V
Digital Output Voltage (SDO) .... –0.3V to (V_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
  LTC1863C/LTC1867C/LTC1867AC .... 0°C to 70°C
  LTC1863I/LTC1867I/LTC1867AI .... –40°C to 85°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 110°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1863CGN
LTC1863IGN
LTC1867CGN
LTC1867IGN
LTC1867ACGN
LTC1867AIGN
GN PART MARKING
1863
1867

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. With external reference (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1863 MIN	LTC1863 TYP	LTC1863 MAX	LTC1867 MIN	LTC1867 TYP	LTC1867 MAX	LTC1867A MIN	LTC1867A TYP	LTC1867A MAX	UNITS
Resolution		●	12			16			16			Bits
No Missing Codes		●	12			15			16			Bits
Integral Linearity Error	Unipolar (Note 7)	●			±1			±4			±2	LSB
	Bipolar	●			±1			±4			±2.5	LSB
Differential Linearity Error		●			±1	–2		3	–1		1.75	LSB
Transition Noise				0.1			0.74			0.74		LSB_{RMS}
Offset Error	Unipolar (Note 8)	●			±3			±32			±32	LSB
	Bipolar	●			±4			±64			±64	LSB
Offset Error Match	Unipolar				±1			±2			±2	LSB
	Bipolar				±1			±2			±2	LSB
Offset Error Drift				±0.5			±0.5			±0.5		ppm/°C
Gain Error	Unipolar				±6			±96			±64	LSB
	Bipolar				±6			±96			±64	LSB
Gain Error Match					±1			±4			±2	LSB
Gain Error Tempco	Internal Reference			±15			±15			±15		ppm/°C
	External Reference			±2.7			±2.7			±2.7		ppm/°C
Power Supply Sensitivity	V_{DD} = 4.75V – 5.25V			±1			±5			±5		LSB

DYNAMIC ACCURACY

(Note 5)

SYMBOL	PARAMETER	CONDITIONS	LTC1863 MIN	LTC1863 TYP	LTC1863 MAX	LTC1867/LTC1867A MIN	LTC1867/LTC1867A TYP	LTC1867/LTC1867A MAX	UNITS
SNR	Signal-to-Noise Ratio	1kHz Input Signal		73.6			89		dB
S/(N+D)	Signal-to-(Noise + Distortion) Ratio	1kHz Input Signal		73.5			88		dB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LTC1863 MIN	LTC1863 TYP	LTC1863 MAX	LTC1867/LTC1867A MIN	LTC1867/LTC1867A TYP	LTC1867/LTC1867A MAX	UNITS
THD	Total Harmonic Distortion	1kHz Input Signal, Up to 5th Harmonic		–94.5			–95		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal		–94.5			–95		dB
	Channel-to-Channel Isolation	100kHz Input Signal		–100			–117		dB
	Full Power Bandwidth	–3dB Point		1.25			1.25		MHz

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1863/LTC1867/LTC1867A MIN	TYP	MAX	UNITS
	Analog Input Range	Unipolar Mode (Note 9) Bipolar Mode	● ●		0-4.096 ±2.048		V V
C_{IN}	Analog Input Capacitance for CH0 to CH7/COM	Between Conversions (Sample Mode) During Conversions (Hold Mode)			32 4		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●	1.5	1.1		µs
	Input Leakage Current	On Channels, CHX = 0V or V_{DD}	●			±1	µA

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS	LTC1863/LTC1867/LTC1867A MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0	2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0		±15		ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V		0.43		mV/V
V_{REF} Output Resistance	$\lvert I_{OUT} \rvert$ ≤0.1mA		6		kΩ
REFCOMP Output Voltage	I_{OUT} = 0		4.096		V

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1863/LTC1867/LTC1867A MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				2		pF
V_{OH}	High Level Output Voltage (SDO)	V_{DD} = 4.75V, I_O = –10µA V_{DD} = 4.75V, I_O = –200µA	 ●	 4	4.75 4.74		V V
V_{OL}	Low Level Output Voltage (SDO)	V_{DD} = 4.75V, I_O = 160µA V_{DD} = 4.75V, I_O = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{SOURCE}	Output Source Current	SDO = 0V			–32		mA
I_{SINK}	Output Sink Current	SDO = V_{DD}			19		mA
	Hi-Z Output Leakage Hi-Z Output Capacitance	$\overline{CS}$/CONV = High, SDO = 0V or V_{DD} $\overline{CS}$/CONV = High (Note 10)	● ●			±10 15	µA pF
	Data Format	Unipolar Bipolar			Straight Binary Two's Complement		

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1863/LTC1867/LTC1867A MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	(Note 9)		4.75		5.25	V
I_{DD}	Supply Current	f_{SAMPLE} = 200ksps NAP Mode SLEEP Mode	● ●		1.3 150 0.2	1.8 3	mA µA µA
P_{DISS}	Power Dissipation		●		6.5	9	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1863/LTC1867/LTC1867A MIN	TYP	MAX	UNITS
f_{SAMPLE}	Maximum Sampling Frequency		●	200			kHz
t_{CONV}	Conversion Time		●		3	3.5	µs
t_{ACQ}	Acquisition Time		●	1.5	1.1		µs
f_{SCK}	SCK Frequency					40	MHz
t_1	$\overline{CS}$/CONV High Time	Short $\overline{CS}$/CONV Pulse Mode	●	40	100		ns
t_2	SDO Valid After SCK↓	C_L = 25pF (Note 11)	●		13	22	ns
t_3	SDO Valid Hold Time After SCK↓	C_L = 25pF	●	5	11		ns
t_4	SDO Valid After $\overline{CS}$/CONV↓	C_L = 25pF	●		10	30	ns
t_5	SDI Setup Time Before SCK↑		●	15	–6		ns
t_6	SDI Hold Time After SCK↑		●	10	4		ns
t_7	SLEEP Mode Wake-Up Time	$C_{REFCOMP}$ = 10µF, C_{VREF} = 2.2µF			60		ms
t_8	Bus Relinquish Time After $\overline{CS}$/CONV↑	C_L = 25pF	●		20	40	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA without latchup.

Note 4: When these pin voltages are taken below GND, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, f_{SAMPLE} = 200ksps at 25°C, $t_r = t_f$ = 5ns and $V_{IN}-$ = 2.5V for bipolar mode unless otherwise specified.

Note 6: Linearity, offset and gain error specifications apply for both unipolar and bipolar modes. The INL and DNL are tested in bipolar mode.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Unipolar offset is the offset voltage measured from +1/2LSB when the output code flickers between 0000 0000 0000 0000 and 0000 0000 0000 0001 for LTC1867 and between 0000 0000 0000 and 0000 0000 0001 for LTC1863. Bipolar offset is the offset voltage measured from –1/2LSB when output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111 for LTC1867, and between 0000 0000 0000 and 1111 1111 1111 for LTC1863.

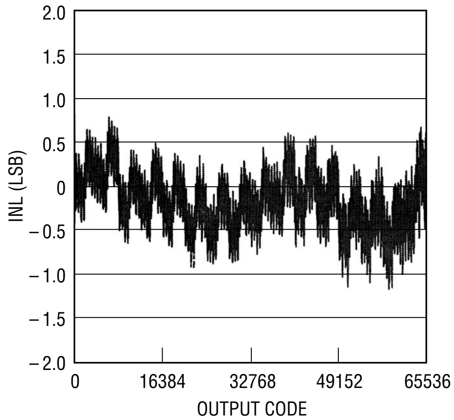
Note 9: Recommended operating conditions. The input range of ±2.048V for bipolar mode is measured with respect to $V_{IN}-$ = 2.5V.

Note 10: Guaranteed by design, not subject to test.

Note 11: t_2 of 25ns maximum allows f_{SCK} up to 20MHz for rising capture with 50% duty cycle and f_{SCK} up to 40MHz for falling capture (with 3ns setup time for the receiving logic).

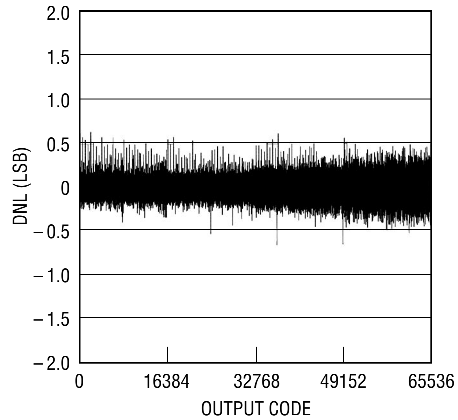
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1867)

Integral Nonlinearity vs Output Code



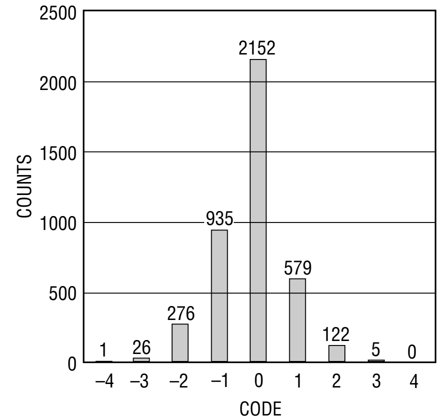
18637 G01

Differential Nonlinearity vs Output Code



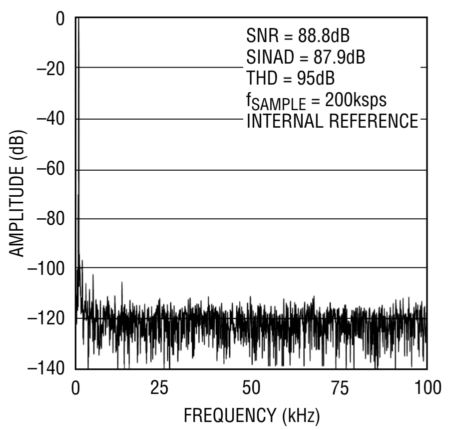
18637 G02

Histogram for 4096 Conversions



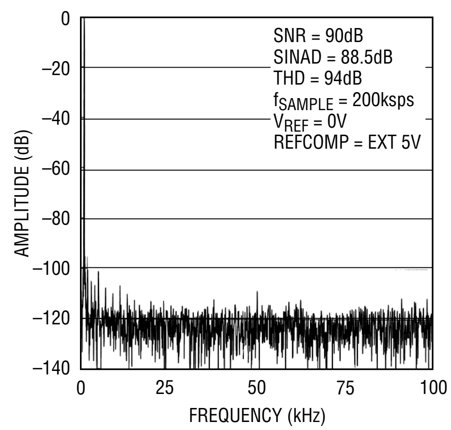
18637 G03

4096 Points FFT Plot (f_{IN} = 1kHz)



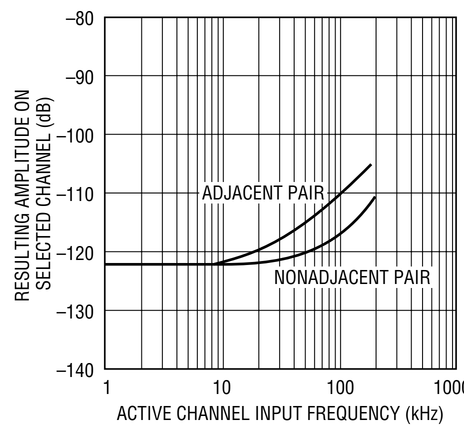
18637 G04

4096 Points FFT Plot (f_{IN} = 1kHz, REFCOMP = External 5V)



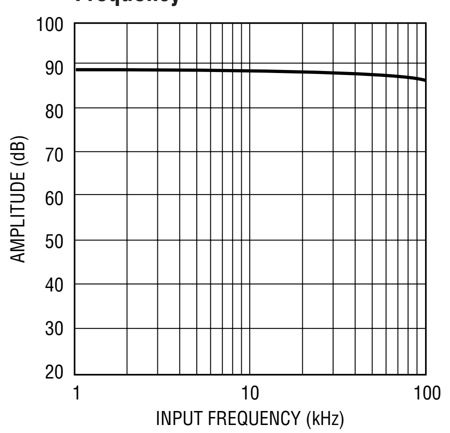
18637 G05

Crosstalk vs Input Frequency



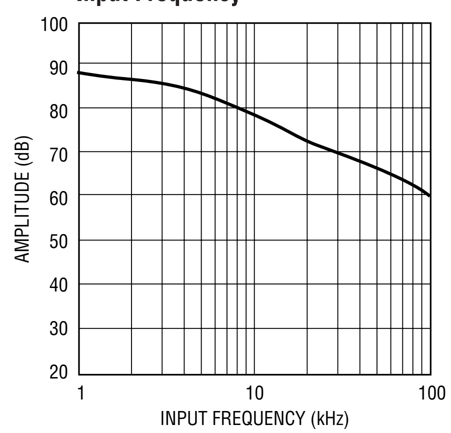
18637 G06

Signal-to-Noise Ratio vs Frequency



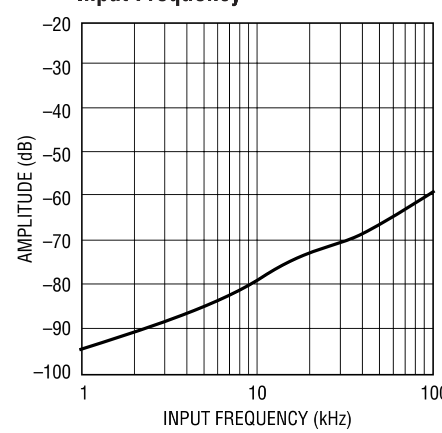
18637 G07

Signal-to-(Noise + Distortion) vs Input Frequency



18637 G08

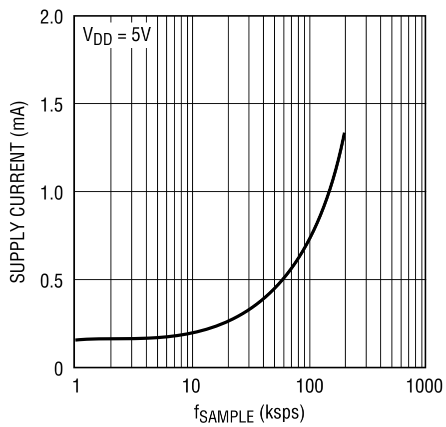
Total Harmonic Distortion vs Input Frequency



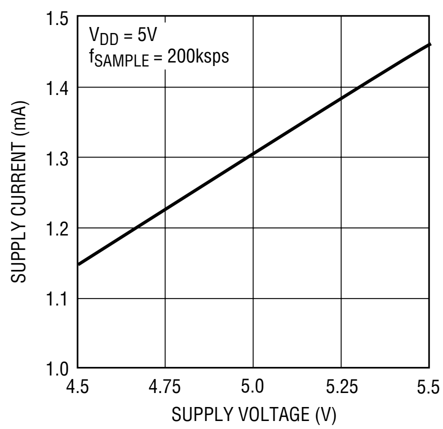
18637 G09

TYPICAL PERFORMANCE CHARACTERISTICS (LTC1863/LTC1867)

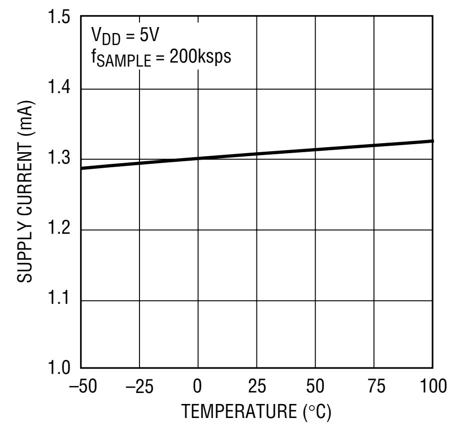
Supply Current vs f_{SAMPLE}



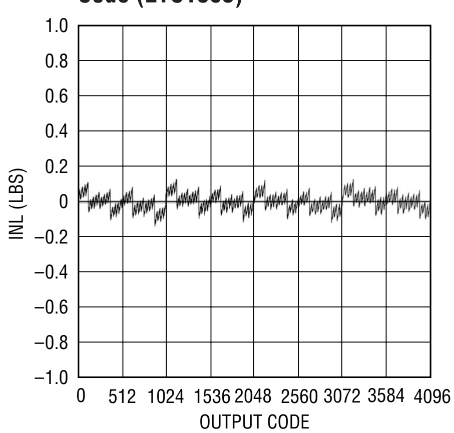
Supply Current vs Supply Voltage



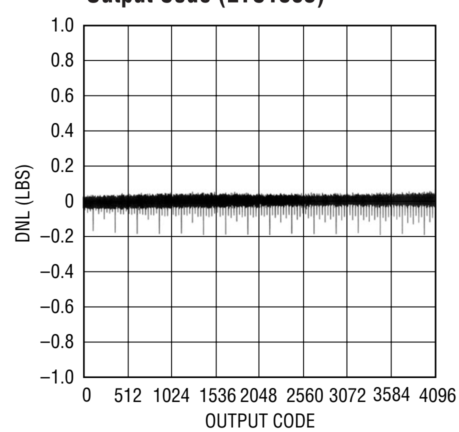
Supply Current vs Temperature



Integral Nonlinearity vs Output Code (LTC1863)



Differential Nonlinearity vs Output Code (LTC1863)



PIN FUNCTIONS

CH0-CH7/COM (Pins 1-8): Analog Input Pins. Analog inputs must be free of noise with respect to GND. CH7/COM can be either a separate channel or the common minus input for the other channels.

REFCOMP (Pin 9): Reference Buffer Output Pin. Bypass to GND with 10μF tantalum capacitor in parallel with 0.1μF ceramic capacitor (4.096V Nominal). To overdrive REFCOMP, tie V_{REF} to GND.

V_{REF} (Pin 10): 2.5V Reference Output. This pin can also be used as an external reference buffer input for improved accuracy and drift. Bypass to GND with 2.2μF tantalum capacitor in parallel with 0.1μF ceramic capacitor.

$\overline{CS}$/CONV (Pin 11): This input provides the dual function of initiating conversions on the ADC and also frames the serial data transfer.

SCK (Pin 12): Shift Clock. This clock synchronizes the serial data transfer.

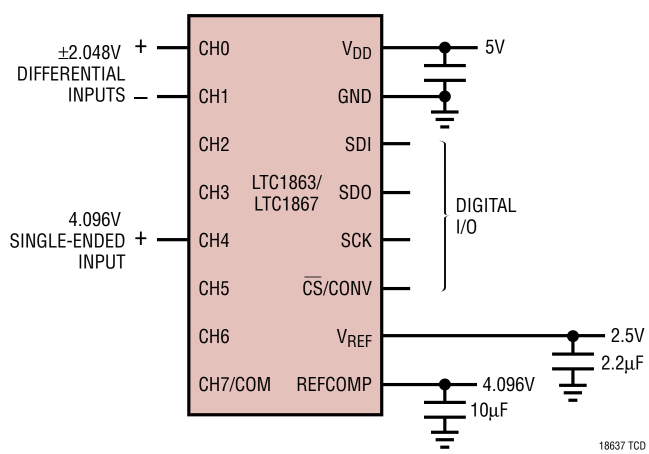
SDO (Pin 13): Digital Data Output. The A/D conversion result is shifted out of this output. Straight binary format for unipolar mode and two's complement format for bipolar mode.

SDI (Pin 14): Digital Data Input Pin. The A/D configuration word is shifted into this input.

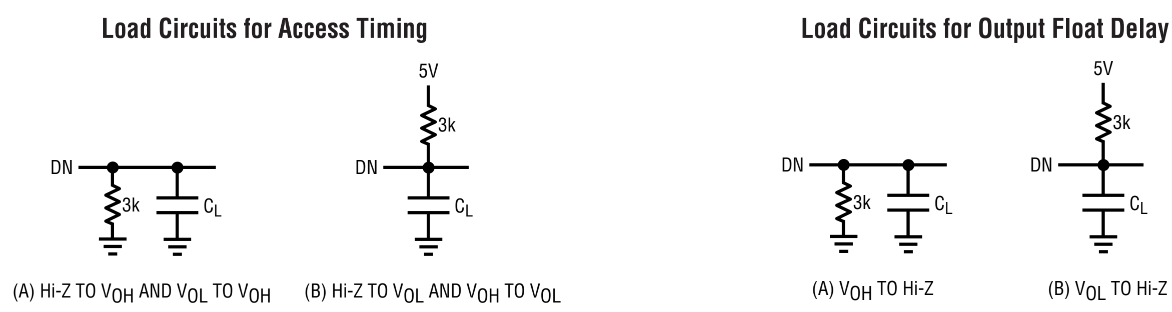
GND (Pin 15): Analog and Digital GND.

V_{DD} (Pin 16): Analog and Digital Power Supply. Bypass to GND with 10μF tantalum capacitor in parallel with 0.1μF ceramic capacitor.

TYPICAL CONNECTION DIAGRAM

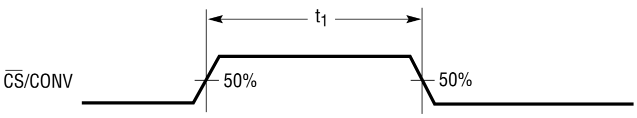


TEST CIRCUITS

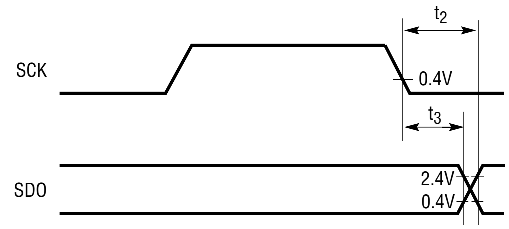


TIMING DIAGRAMS

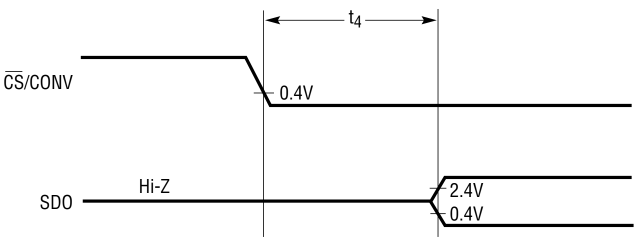
t_1 (For Short Pulse Mode)



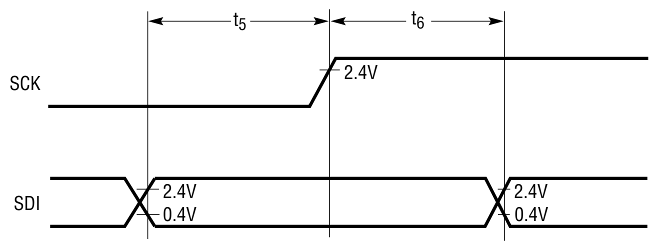
t_2 (SDO Valid Before SCK↑),
t_3 (SDO Valid Hold Time After SCK↓)



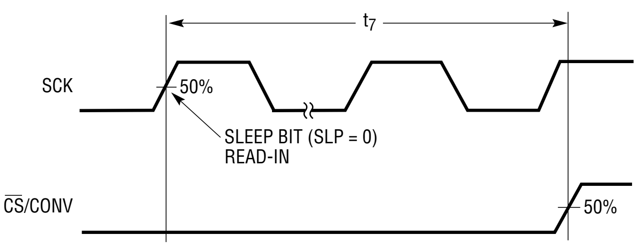
t_4 (SDO Valid After CONV↓)



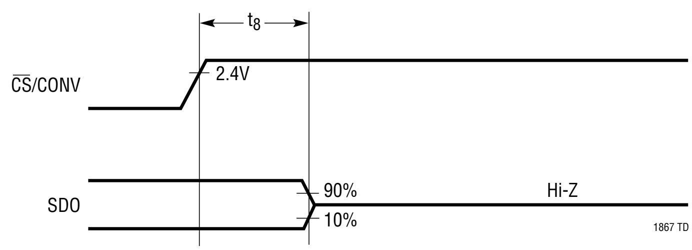
t_5 (SDI Setup Time Before SCK↑),
t_6 (SDI Hold Time After SCK↑)



t_7 (SLEEP Mode Wake-Up Time)



t_8 (BUS Relinquish Time)



APPLICATIONS INFORMATION

Overview

The LTC1863/LTC1867 are complete, low power multiplexed ADCs. They consist of a 12-/16-bit, 200ksps capacitive successive approximation A/D converter, a precision internal reference, a configurable 8-channel analog input multiplexer (MUX) and a serial port for data transfer.

Conversions are started by a rising edge on the $\overline{CS}$/CONV input. Once a conversion cycle has begun, it cannot be restarted. Between conversions, the ADCs receive an input word for channel selection and output the conversion result, and the analog input is acquired in preparation for the next conversion. In the acquire phase, a minimum time of 1.5μs will provide enough time for the sample-and-hold capacitors to acquire the analog signal.

During the conversion, the internal differential 16-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). The input is sucessively compared with the binary weighted charges supplied by the differential capacitive DAC. Bit decisions are made by a low-power, differential comparator. At the end of a conversion, the DAC output balances the analog input. The SAR contents (a 12-/16-bit data word) that represent the analog input are loaded into the 12-/16-bit output latches.

APPLICATIONS INFORMATION

Analog Input Multiplexer

The analog input multiplexer is controlled by a 7-bit input data word. The input data word is defined as follows:

SD	OS	S1	S0	COM	UNI	SLP

SD = SINGLE/$\overline{\text{DIFFERENTIAL}}$ BIT

OS = ODD/$\overline{\text{SIGN}}$ BIT

S1 = ADDRESS SELECT BIT 1

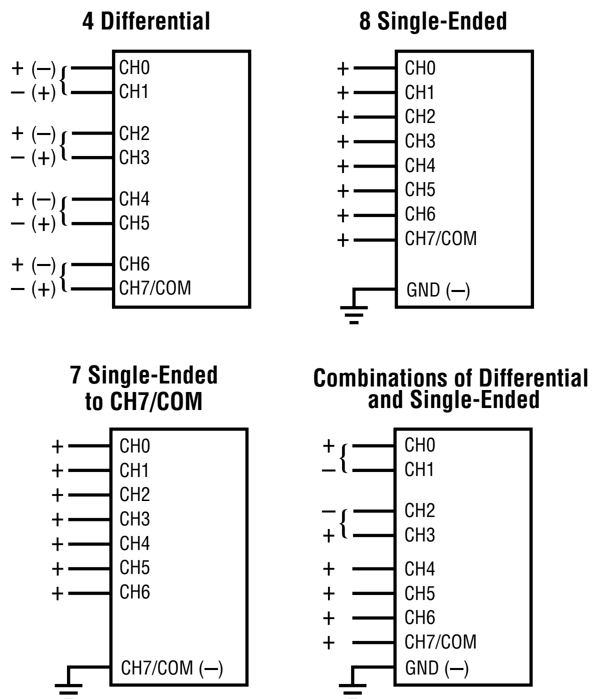
S0 = ADDRESS SELECT BIT 0

COM = CH7/COM CONFIGURATION BIT

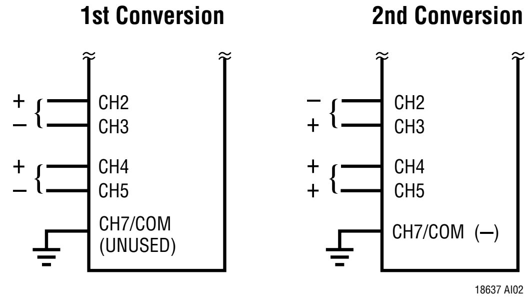
UNI = UNIPOLAR/$\overline{\text{BIPOLAR}}$ BIT

SLP = SLEEP MODE BIT

Examples of Multiplexer Options



Changing the MUX Assignment "On the Fly"



Tables 1 and 2 show the configurations when COM = 0, and COM = 1.

Table 1. Channel Configuration (When COM = 0, CH7/COM Pin Is Used as CH7)

SD	OS	S1	S0	COM	Channel Configuration "+"	"-"
0	0	0	0	0	CH0	CH1
0	0	0	1	0	CH2	CH3
0	0	1	0	0	CH4	CH5
0	0	1	1	0	CH6	CH7
0	1	0	0	0	CH1	CH0
0	1	0	1	0	CH3	CH2
0	1	1	0	0	CH5	CH4
0	1	1	1	0	CH7	CH6
1	0	0	0	0	CH0	GND
1	0	0	1	0	CH2	GND
1	0	1	0	0	CH4	GND
1	0	1	1	0	CH6	GND
1	1	0	0	0	CH1	GND
1	1	0	1	0	CH3	GND
1	1	1	0	0	CH5	GND
1	1	1	1	0	CH7	GND

Table 2. Channel Configuration (When COM = 1, CH7/COM Pin Is Used as COMMON)

SD	OS	S1	S0	COM	Channel Configuration "+"	"-"
1	0	0	0	1	CH0	CH7/COM
1	0	0	1	1	CH2	CH7/COM
1	0	1	0	1	CH4	CH7/COM
1	0	1	1	1	CH6	CH7/COM
1	1	0	0	1	CH1	CH7/COM
1	1	0	1	1	CH3	CH7/COM
1	1	1	0	1	CH5	CH7/COM

APPLICATIONS INFORMATION

Driving the Analog Inputs

The analog inputs of the LTC1863/LTC1867 are easy to drive. Each of the analog inputs can be used as a single-ended input relative to the GND pin (CH0-GND, CH1-GND, etc) or in pairs (CH0 and CH1, CH2 and CH3, CH4 and CH5, CH6 and CH7) for differential inputs. In addition, CH7 can act as a COM pin for both single-ended and differential modes if the COM bit in the input word is high. Regardless of the MUX configuration, the "+" and "–" inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors during the acquire mode. In conversion mode, the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low then the LTC1863/LTC1867 inputs can be driven directly. More acquisition time should be allowed for a higher impedance source.

The following list is a summary of the op amps that are suitable for driving the LTC1863/LTC1867. More detailed information is available in the Linear Technology data books or Linear Technology website.

LT1007 - Low noise precision amplifier. 2.7mA supply current ±5V to ±15V supplies. Gain bandwidth product 8MHz. DC applications.

LT1097 - Low cost, low power precision amplifier. 300μA supply current. ±5V to ±15V supplies. Gain bandwidth product 0.7MHz. DC applications.

LT1227 - 140MHz video current feedback amplifier. 10mA supply current. ±5V to ±15V supplies. Low noise and low distortion.

LT1360 - 37MHz voltage feedback amplifier. 3.8mA supply current. ±5V to ±15V supplies. Good AC/DC specs.

LT1363 - 50MHz voltage feedback amplifier. 6.3mA supply current. Good AC/DC specs.

LT1364/LT1365 - Dual and quad 50MHz voltage feedback amplifiers. 6.3mA supply current per amplifier. Good AC/DC specs.

LT1468 - 90MHz, 22V/μs 16-bit accurate amplifier

LT1469 - Dual LT1468

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1863/LTC1867 noise and distortion. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For instance, Figure 1 shows a 50Ω source resistor and a 2000pF capacitor to ground on the input will limit the input bandwidth to 1.6MHz. The source impedance has to be kept low to avoid gain error and degradation in the AC performance. The capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

APPLICATIONS INFORMATION

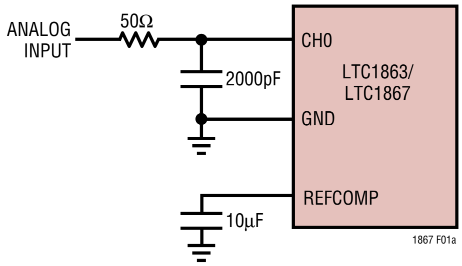


Figure 1a. Optional RC Input Filtering for Single-Ended Input

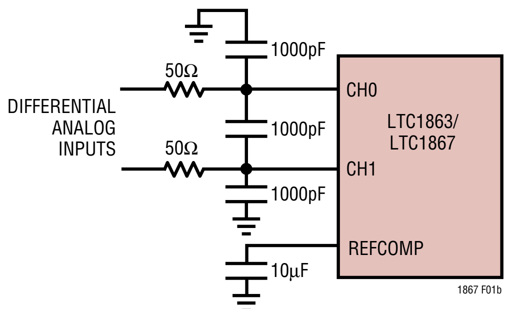


Figure 1b. Optional RC Input Filtering for Differential Inputs

DC Performance

One way of measuring the transition noise associated with a high resolution ADC is to use a technique where a DC signal is applied to the input of the ADC and the resulting output codes are collected over a large number of conversions. For example, in Figure 2 the distribution of output codes is shown for a DC input that had been digitized 4096 times. The distribution is Gaussian and the RMS code transition noise is about 0.74LSB.

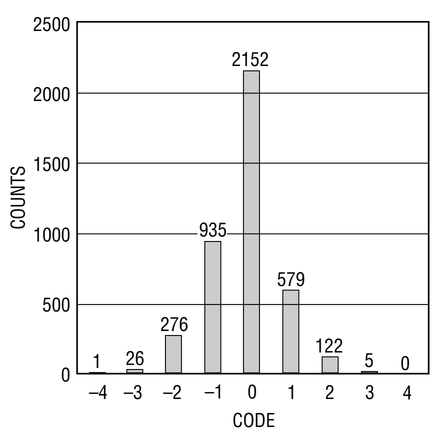


Figure 2. LTC1867 Histogram for 4096 Conversions

Dynamic Performance

FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental.

Signal-to-Noise Ratio

The Signal-to-Noise and Distortion Ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 3 shows a typical SINAD of 87.9dB with a 200kHz sampling rate and a 1kHz input. When an external 5V is applied to REFCOMP (tie V_{REF} to GND), a signal-to-noise ratio of 90dB can be achieved.

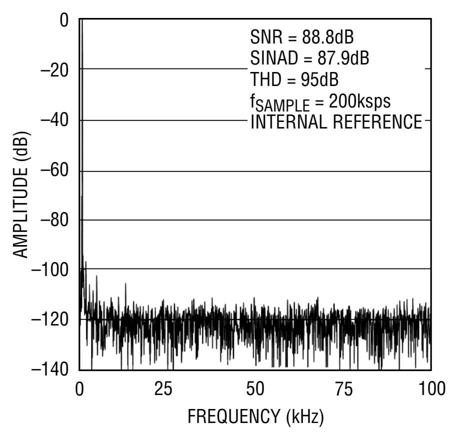


Figure 3. LTC1867 Nonaveraged 4096 Point FFT Plot

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

APPLICATIONS INFORMATION

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

Internal Reference

The LTC1863/LTC1867 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.5V. It is internally connected to a reference amplifier and is available at V_{REF} (Pin 10). A 6k resistor is in series with the output so that it can be easily overdriven by an external reference if better drift and/or accuracy are required as shown in Figure 4. The reference amplifier gains the V_{REF} voltage by 1.638V to 4.096V at REFCOMP (Pin 9). This reference amplifier compensation pin, REFCOMP, must be bypassed with a 10µF ceramic or tantalum in parallel with a 0.1µF ceramic for best noise performance.

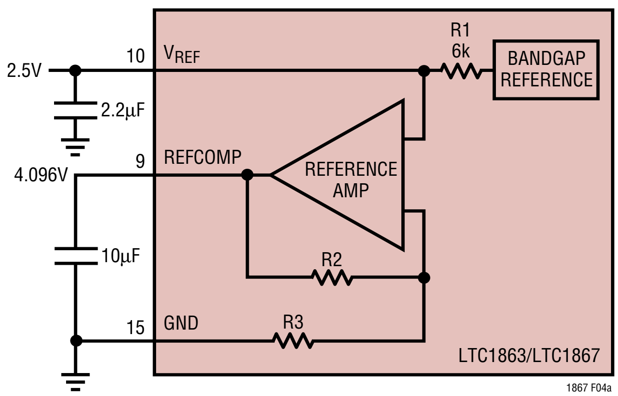


Figure 4a. LT1867 Reference Circuit

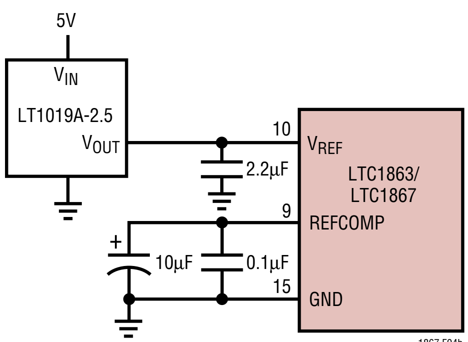


Figure 4b. Using the LT1019-2.5 as an External Reference

Digital Interface

The LTC1863/LTC1867 have very simple digital interface that is enabled by the control input, $\overline{CS}$/CONV. A logic rising edge applied to the $\overline{CS}$/CONV input will initiate a conversion. After the conversion, taking $\overline{CS}$/CONV low will enable the serial port and the ADC will present digital data in two's complement format in bipolar mode or straight binary format in unipolar mode, through the SCK/SDO serial port.

Internal Clock

The internal clock is factory trimmed to achieve a typical conversion time of 3µs and a maximum conversion time, 3.5µs, over the full operating temperature range. The typical acquisition time is 1.1µs, and a throughput sampling rate of 200ksps is tested and guaranteed.

Automatic Nap Mode

The LTC1863/LTC1867 go into automatic nap mode when $\overline{CS}$/CONV is held high after the conversion is complete. With a typical operating current of 1.3mA and automatic 150µA nap mode between conversions, the power dissipation drops with reduced sample rate. The ADC only keeps the V_{REF} and REFCOMP voltages active when the part is in the automatic nap mode. The slower the sample rate allows the power dissipation to be lower (see Figure 5).

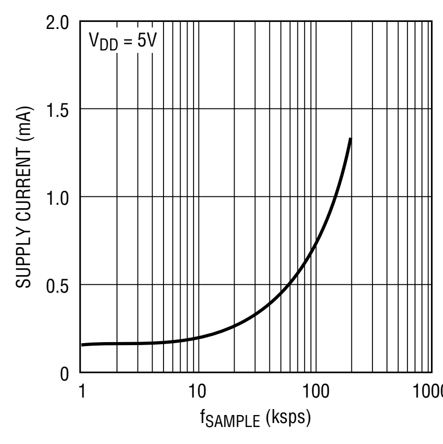


Figure 5. Supply Current vs f_{SAMPLE}

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If the $\overline{CS}$/CONV returns low during a bit decision, it can create a small error. For best performance ensure that the $\overline{CS}$/CONV returns low either within 100ns after the conversion starts (i.e. before the first bit decision) or after the conversion ends. If $\overline{CS}$/CONV is low when the conversion ends, the MSB bit will appear on SDO at the end of the conversion and the ADC will remain powered up.

Sleep Mode

If the SLP = 1 is selected in the input word, the ADC will enter SLEEP mode and draw only leakage current (provided that all the digital inputs stay at GND or V_{DD}). After release from the SLEEP mode, the ADC need 60ms to wake up (2.2µF/10µF bypass capacitors on V_{REF}/REFCOMP pins).

Broad Layout and Bypassing

To obtain the best performance, a printed circuit board with a ground plane is required. Layout for the printed circuit board should ensure digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital signal alongside an analog signal.

All analog inputs should be screened by GND. V_{REF}, REFCOMP and V_{DD} should be bypassed to this ground plane as close to the pin as possible; the low impedance of the common return for these bypass capacitors is essential to the low noise operation of the ADC. The width for these tracks should be as wide as possible.

Timing and Control

Conversion start is controlled by the $\overline{CS}$/CONV digital input. The rising edge transition of the $\overline{CS}$/CONV will start a conversion. Once initiated, it cannot be restarted until the conversion is complete. Figures 6 and 7 show the timing diagrams for two types of $\overline{CS}$/CONV pulses.

Example 1 (Figure 6) shows the LTC1863/LTC1867 operating in automatic nap mode with $\overline{CS}$/CONV signal staying HIGH after the conversion. Automatic nap mode provides power reduction at reduced sample rate. The ADCs can also operate with the $\overline{CS}$/CONV signal returning LOW before the conversion ends. In this mode (Example 2, Figure 7), the ADCs remain powered up.

Figures 8 and 9 are the transfer characteristics for the bipolar and unipolar mode.

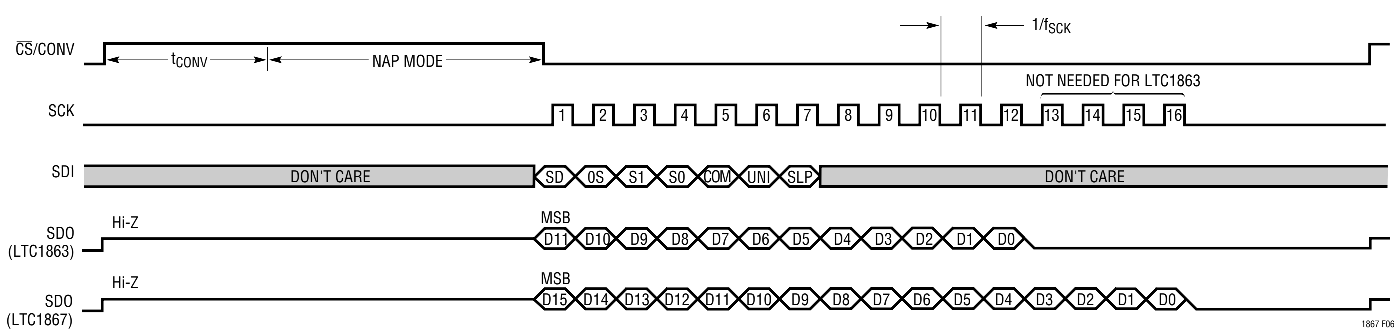


Figure 6. Example 1, $\overline{CS}$/CONV Starts a Conversion and Remains HIGH Until Next Data Transfer. With $\overline{CS}$/CONV Remaining HIGH after the Conversion, Automatic Nap Modes Provides Power Reduction at Reduced Sample Rate.

APPLICATIONS INFORMATION

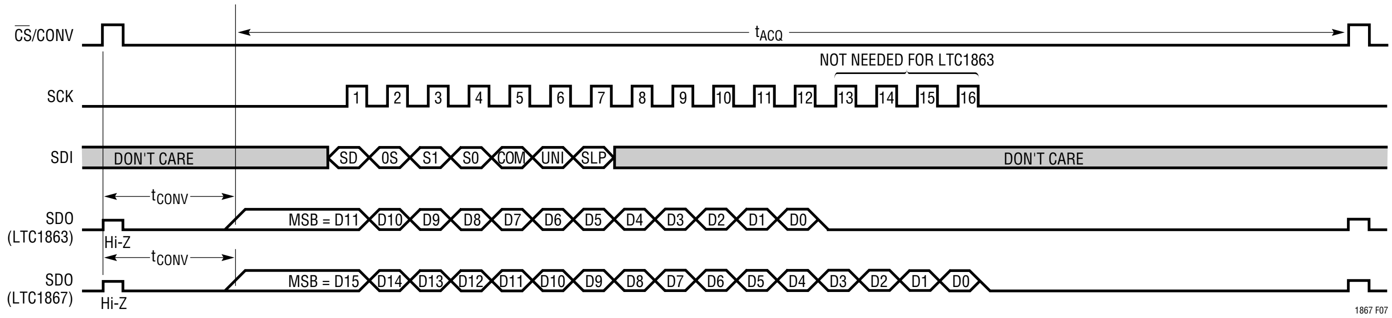


Figure 7. Example 2, $\overline{CS}$/CONV Starts a Conversion with Short Active HIGH Pulse. With $\overline{CS}$/CONV Returning LOW Before the Conversion, the ADC Remains Powered Up.

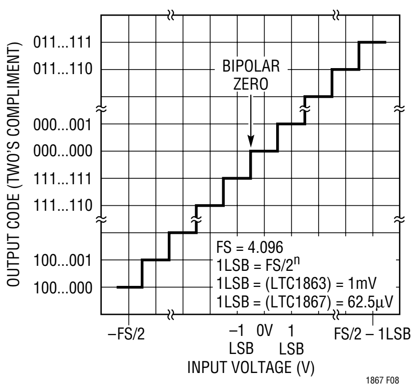


Figure 8. LTC1863/LTC1867 Bipolar Transfer Characteristics (Two's Complement)

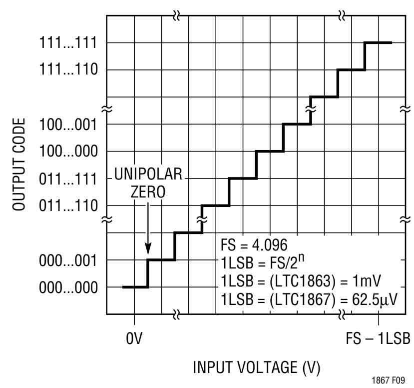
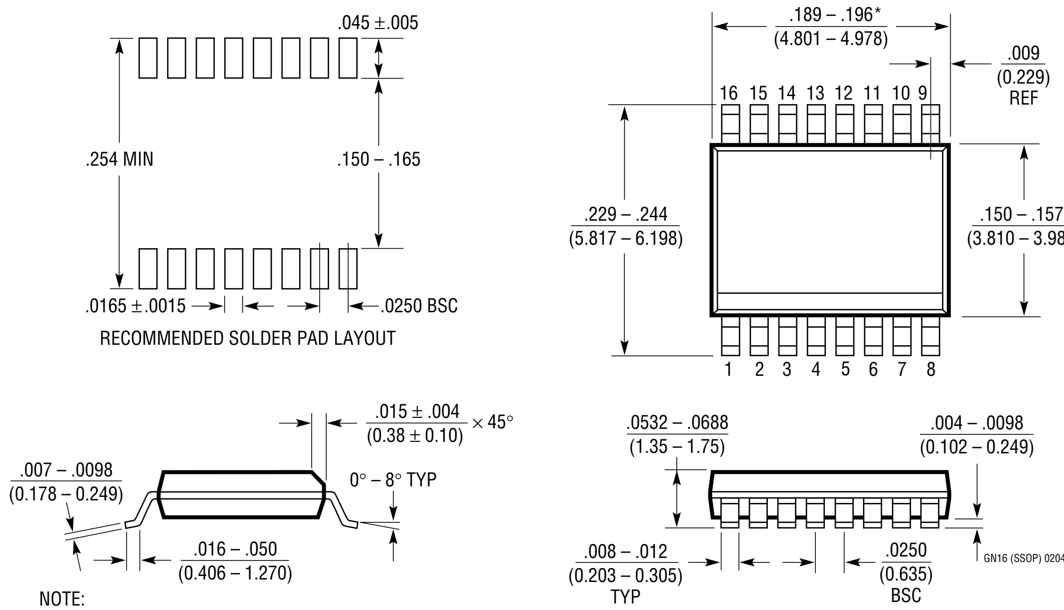


Figure 9. LTC1863/LTC1867 Unipolar Transfer Characteristics (Straight Binary)

PACKAGE DESCRIPTION

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1417	14-Bit, 400ksps Serial ADC	20mW, Unipolar or Bipolar, Internal Reference, SSOP-16 Package
LT1460	Micropower Precision Series Reference	Bandgap, 130µA Supply Current, 10ppm/°C, SOT-23 Package
LT1468/LT1469	Single/Dual 90MHz, 22V/µs, 16-Bit Accurate Op Amps	Low Input Offset: 75µV/125µV
LTC1609	16-Bit, 200ksps Serial ADC	65mW, Configurable Bipolar and Unipolar Input Ranges, 5V Supply
LT1790	Micropower Low Dropout Reference	60µA Supply Current, 10ppm/°C, SOT-23 Package
LTC1850/LTC1851	10-Bit/12-Bit, 8-Channel, 1.25Msps ADC	Parallel Output, Programmable MUX and Sequencer, 5V Supply
LTC1852/LTC1853	10-Bit/12-Bit, 8-Channel, 400ksps ADC	Parallel Output, Programmable MUX and Sequencer, 3V or 5V Supply
LTC1860/LTC1861	12-Bit, 1-/2-Channel 250ksps ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1860L/LTC1861L	3V, 12-Bit, 1-/2-Channel 150ksps ADC	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages
LTC1864/LTC1865	16-Bit, 1-/2-Channel 250ksps ADC in MSOP	850µA at 250ksps, 2µA at 1ksps, SO-8 and MSOP Packages
LTC1864L/LTC1865L	3V, 16-Bit, 1-/2-Channel 150ksps ADC in MSOP	450µA at 150ksps, 10µA at 1ksps, SO-8 and MSOP Packages

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